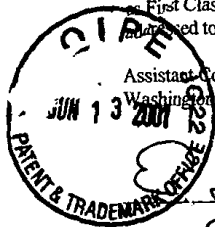


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Washington, D.C. 20231



Date: 7 June 2001

2818
#3

PATENT

Attorney Docket No.: DB000575-010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Keeth, et al.)	Examiner: Not yet assigned
Serial No.: 08/801,628)	Art Unit: 2818
Filed: 08 March 2001)	
Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY)	

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TC 2800 MAIL ROOM

TRANSMITTAL FOR INFORMATION DISCLOSURE STATEMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In regards to the above-referenced patent application, transmitted herewith for filing are:

1. an Information Disclosure Statement By Applicant (Form PTO/SB/08A);
2. an Information Disclosure Statement By Applicant (Form PTO/SB/08B) (two pages); and
3. a copy of each of the thirty-three (33) references listed on Forms PTO/SB/08A and PTO/SB/08B.

Also enclosed is a return postcard. Please date stamp the postcard and return it to us to acknowledge receipt of this information disclosure statement.



The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to our Deposit Account No. 20-0888. A duplicate copy of this Transmittal letter is enclosed.

Respectfully submitted,

Edward L. Pencoske
Reg. No. 29,688
THORP REED & ARMSTRONG, LLP
One Oxford Centre
301 Grant Street, 14th Floor
Pittsburgh, PA 15219-1425
(412) 394-7789

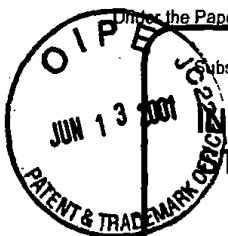
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete if Known

Application Number 08/801,628
Filing Date 08 March 2001
First Named Inventor Keeth et al.
Group Art Unit 2818
Examiner Name Not yet assigned
Attorney Docket Number DB000575-010

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
		6,043,118		Suwanai et al.	03/28/2000	
		5,960,455		Bauman	09/28/1999	
		5,838,627		Tomishima et al.	11/17/1998	
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		5,651,011		Keeth	07/22/1997	
		5,614,859		Onq	03/25/1997	
		5,574,697		Manning	11/12/1996	
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		5,552,739		Keeth et al.	09/03/1996	
		5,526,364		Roohparvar	06/11/1996	
		5,519,360		Keeth	05/21/1996	
		5,481,179		Keeth	01/02/1996	
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		5,373,227		Keeth	12/13/1994	
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		5,231,605		Lee	07/27/1993	
		5,212,440		Waller	05/18/1993	
		5,159,273		Wright et al.	10/27/1992	
		5,155,704		Walther et al.	10/13/1992	
		4,970,725		McEnroe et al.	11/13/1990	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				

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Date
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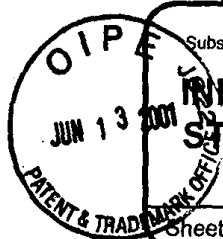
¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 3

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Application Number	08/801,628
Filing Date	08 March 2001
First Named Inventor	Keeth et al.
Group Art Unit	2818
Examiner Name	Not yet assigned
Attorney Docket Number	DB000575-010

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SUGIBAYASHI ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		TAGUCHI ET AL., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26 (No. 11), (November 1991)	
		KITSUKAWA ET AL., "256-Mb DRAM Circuit Technologies for File Applications", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		JEDEC SOLID STATE PRODUCTS ENGINEERING COUNCIL, "Committee Letter Ballot", JC-42.3-95-73, Item #633.13, Arlington, VA (April 1995)	
		YOO ET AL., "SP 23.6: A 32-Bank 1Gb DRAM with 1 GB/s Bandwidth", ISSCC96/Session 23/DRAM/PAPER SP 23.6	
		NITTA ET AL., "SP 23.5: A 1.6GB/s Data-Rate 1Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block and Distributed Bank Architecture", ISSCC96/Session 23/DRAM PAPER SP 23.5	
		U.S. Patent Application S.N. 08/521,563, entitled IMPROVED VOLTAGE REGULATOR CIRCUIT, filed 8/30/95	
		U.S. Patent Application S.N. 08/668,347, entitled DIFFERENTIAL VOLTAGE REGULATOR, filed 6/26/96	
		U.S. Patent Application S.N. 08/460,234, entitled SINGLE DEPOSITION LAYER METAL DYNAMIC RANDOM ACCESS MEMORY, filed 8/17/95	
		U.S. Patent Application S.N. 08/420,943, entitled DYNAMIC RANDOM-ACCESS MEMORY, filed 6/4/95	
		U.S. Patent Application S.N. 08/194,184, entitled INTEGRATED CIRCUIT POWER SUPPLY HAVING PIECEWISE LINEARITY, filed 2/8/94	

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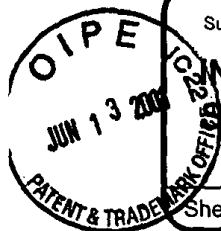
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Sheet 3 of 3

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Application Number	08/801,628
Filing Date	03/08/2001
First Named Inventor	Keeth et al.
Group Art Unit	2818
Examiner Name	Not yet assigned
Attorney Docket Number	DB000575-010

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		U.S. Patent Application S.N. 08/137,679, entitled A VOLTAGE REFERENCE CIRCUIT WITH COMMON GATE LOADING FOR A CURRENT MIRROR OUTPUT STAGE, filed 10/14/93	
		U.S. Patent Application S.N. 08/325,766, entitled AN EFFICIENT METHOD FOR OBTAINING USABLE PARTS FROM A PARTIALLY GOOD MEMORY INTEGRATED CIRCUIT, filed 10/19/94	

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